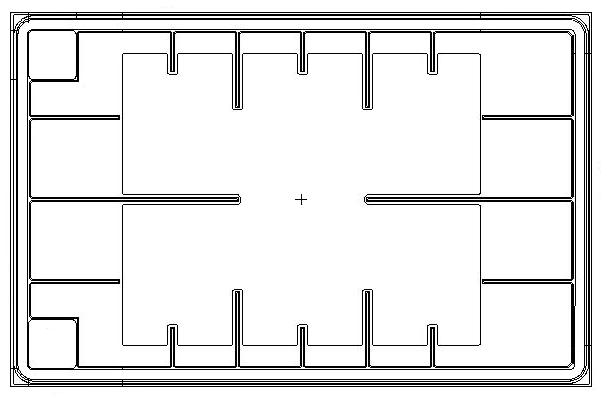
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**G**

**G**

**+ S**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: G = .0046” X .0046”**

**Backside Potential:**

**Mask Ref: IX86**

**APPROVED BY: DK DIE SIZE .355” X .550” DATE: 7/21/21**

**MFG: IXYS THICKNESS .010” P/N: IXFD26N100P-86**

**DG 10.1.2**

#### Rev B, 7/19/02